



Z8400/84C00

NMOS/CMOS Z80 CPU

CENTRAL PROCESSING UNIT

FEATURES

- The Extensive Instruction Set. Contains 158 Instructions, Including the 8080A Instructions Set as a Subset.
- Single 5 Volt Power Supply
- NMOS Version for Low Cost, High Performance Solutions; CMOS Version for High Performance, Low Power Designs.
- NMOS Z084004 - 4 MHz
Z0840006 - 6.17 MHz
Z084008 - 8 MHz
- CMOS Z0840006 - DC to 6.17 MHz
Z84C0008 - DC to 8 MHz
Z84C0010 - DC to 10 MHz
Z84C0020 - DC to 20 MHz
- 6 MHz Version can be Operated at 6.144 MHz Clock Speed
- The Z80 Microprocessors and Associated Family of Peripherals can be Linked by a Vectored Interrupt System. This System can be Daisy-Chain'd to Allow Implementation of a Priority Interrupt Scheme.
- Duplicate Set of Both General-Purpose and Flag Registers
- Two 16-Bit Index Registers
- Three Modes of Maskable Interrupts:
 - Mode 0 - 8080A Similar
 - Mode 1 - Non-Z80 Environment, Location 38H
 - Mode 2 - Z80 Family Peripherals, Vectored Interrupts
- On-Chip Dynamic Memory Refresh Counter

GENERAL DESCRIPTION

The Z8400/Z84C00 CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The speed offerings from 6 - 20 MHz suit a wide range of applications which migrate software. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of

"Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers.

GENERAL DESCRIPTION (Continued)

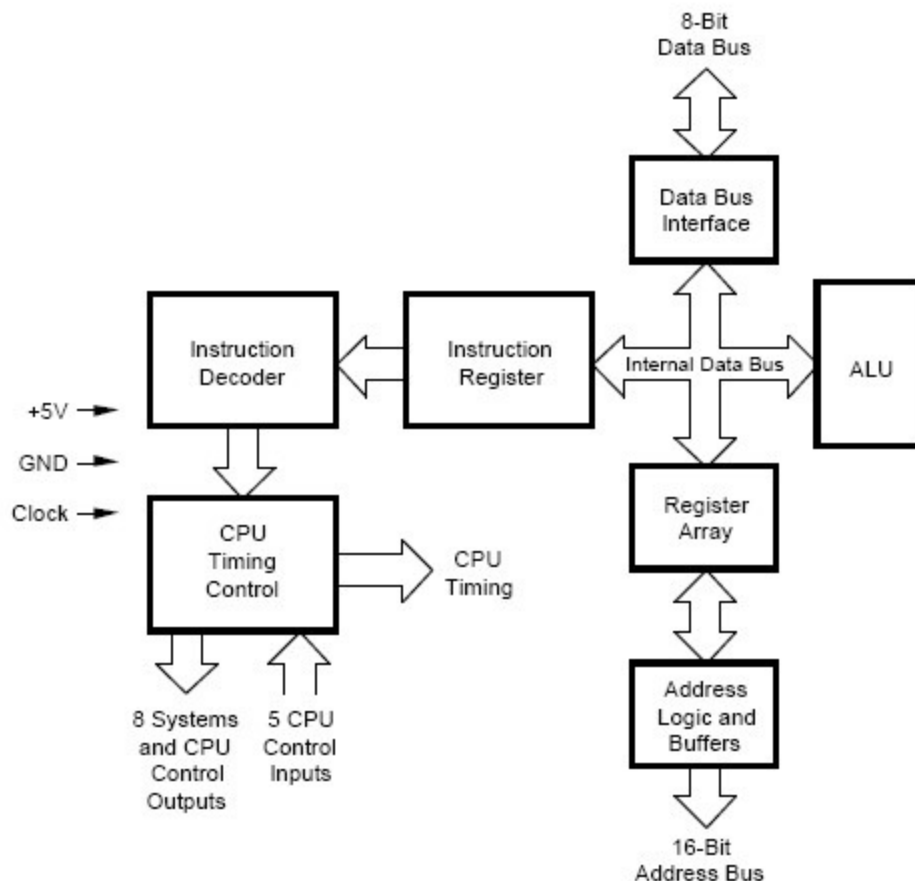


Figure 1. Z8400/C00 Functional Block Diagram

© 1997 by Zilog, Inc. All rights reserved. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Zilog, Inc. The information in this document is subject to change without notice. Devices sold by Zilog, Inc. are covered by warranty and patent indemnification provisions appearing in Zilog, Inc. Terms and Conditions of Sale only.

ZILOG, INC. MAKES NO WARRANTY, EXPRESS, STATUTORY, IMPLIED OR BY DESCRIPTION, REGARDING THE INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED DEVICES FROM INTELLECTUAL PROPERTY INFRINGEMENT. ZILOG, INC. MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE.

Zilog, Inc. shall not be responsible for any errors that may appear in this document. Zilog, Inc. makes no commitment to update or keep current the information contained in this document.

Zilog's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the customer and Zilog prior to use. Life support devices or systems are those which are intended for surgical implantation into the body, or which sustains life whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-8800
Telephone (408) 370-8000
Telex 910-338-7821
FAX 408 370-8056
Internet: <http://www.zilog.com>