4. TMS9118/9128/9129 ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)†

Supply voltage, V_{CC}	−0.3 V to 20 V
All input voltages	−0.3 V to 20 V
Output voltage	−2 V to 7 V
Continuous power dissipation	1.3 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

† Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4.2 RECOMMENDED OPERATING CONDITIONS†

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}‡		4.75		5.25	V
Supply voltage, V_{SS}‡			0		V
Input voltage, V_I, $\overline{RESET}$/SYNC pin	SYNC active	10		12	V
	$\overline{RESET}$ active			0.8	V
	SYNC and $\overline{RESET}$ inactive	3.5		6	
High-level input voltage, V_{IH}	XTAL1, XTAL2	2.75			V
	All other inputs	2.2			
Low-level input voltage, V_{IL}	XTAL1, XTAL2			0.6	V
	All other inputs			0.8	
Operating free-air temperature, T_A		0		70	°C

† All voltage values are with respect to V_{SS}.
‡ A 10 μF to 50 μF decoupling capacitor is suggested between V_{CC} and V_{SS} to guarantee proper VDP operation and minimize noise from the power supply.

4.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$	I_{OH} = 400 μA	2.7	3.4		V
		All other outputs		2.4	3.2		
V_{OL}	Low-level output voltage	CPU data	I_{OL} = 1.2 mA		0.3	0.6	V
		DRAM interface	I_{OL} = −800 μA		0.3	0.6	
I_{OZH}	Off-state output current, high-level voltage applied	CD0-CD7 outputs	V_O = 5.25 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied	CD0-CD7 outputs	V_O = 0.4 V			−100	μA
I_{IH}	High-level input current		V_I = 5.25 V, All other pins = 0 V			10	μA
I_{IL}	Low-level input current		V_I = 0 V, All other pins = 5.25 V			−10	μA

4.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED) (Concluded)

TMS9118/9128/9129 (Figure 4-1)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{WHITE}	White voltage level	COMVID or Y	R_L = 470 Ω, C_L = 75 pF		3.1		V
V_{BLACK}	Black voltage level	COMVID or Y			2.1		V
V_{SYNC}	Sync voltage level	COMVID or Y			1.7		V
V_{WMB}	Voltage difference, $V_{WHITE} - V_{BLACK}$	COMVID or Y		0.8	1		V
V_{BMS}	Voltage difference, $V_{BLACK} - V_{SYNC}$	COMVID (TMS9118 only)		320	400		mV
		Y (TMS9128 only)		370	450		
		Y (TMS9129 only)		345	425		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

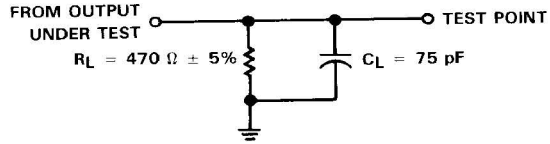


FIGURE 4-1 – TMS9118/9128/9129 LOAD CIRCUIT FOR COMVID AND R-Y, Y, B-Y SWITCHING CHARACTERISTICS

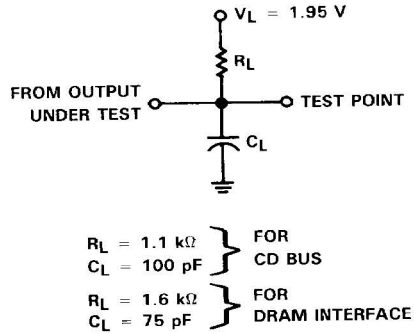


FIGURE 4-2 – TMS9118/9128/9129 LOAD CIRCUIT FOR ALL OUTPUTS EXCEPT COMVID, R-Y, Y, B-Y

4.4 TIMING REQUIREMENTS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS FOR TMS9118/9128/9129

CPU-VDP Interface (Figures 4-3 and 4-4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(ARL)}$	Address setup time before $\overline{CSR}$ low		0		ns
$t_{su(AWL)}$	Address setup time before $\overline{CSW}$ low		30		ns
$t_{h(WLA)}$	Address hold time after $\overline{CSW}$ low		30		ns
$t_{su(DWH)}$	Data setup time before $\overline{CSW}$ high		100		ns
$t_{h(WHD)}$	Data hold time after $\overline{CSW}$ high		30		ns
$t_{w(WL)}$	Pulse duration, $\overline{CSW}$ low		200		ns

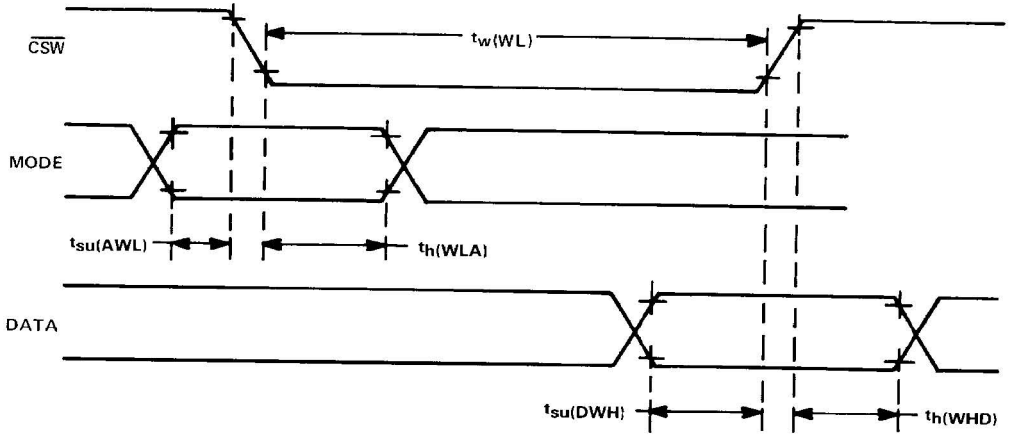
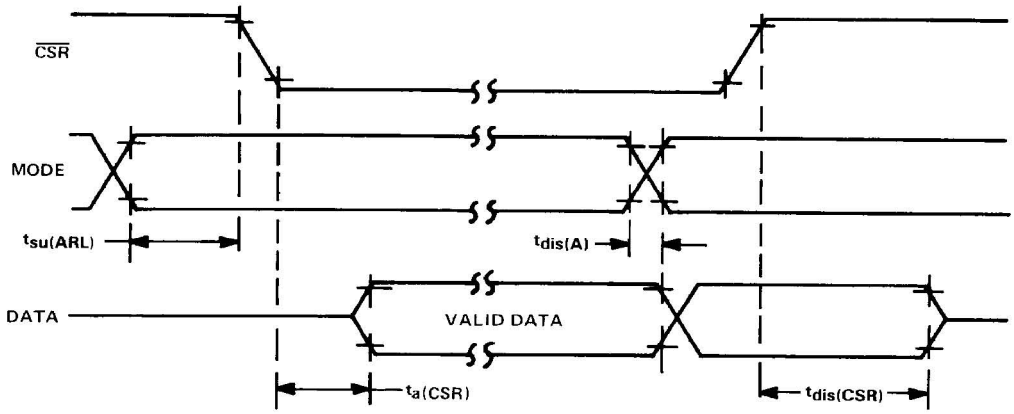


FIGURE 4-3 – CPU-VDP WRITE CYCLE FOR TMS9118/9128/9129

4.4 TIMING REQUIREMENTS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS FOR TMS9118/9128/9129 (Continued)



NOTE: All measurements are made at 10% and 90% points.

FIGURE 4-4 – CPU-VDP READ CYCLE FOR TMS9118/9128/9129

NOTE

For register and memory read/write cycle times refer to timing requirements given in electrical specifications.

VDP-VRAM Interface

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(DCH)}$	Input data setup time before $\overline{CAS}$ high	60			ns
$t_{h(CHD)}$	Input data hold time after $\overline{CAS}$ high	0			ns

Register and Memory Access Cycle Times

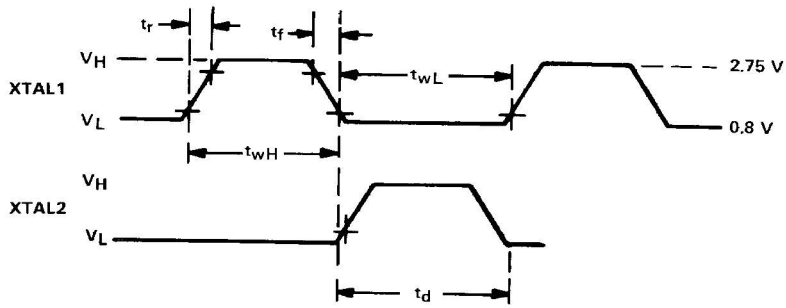
PARAMETER			MIN	NOM	MAX	UNIT
$t_{c(REG)}$	Cycle time between registers read or write windows		2		2	μs
$t_{c(MEM)}$	Cycle time between memory read or write windows	Blanked screen	2		2	μs
		Vertical retrace (4.3 ms after Int.)	2		2	μs
		Text (Active area)	2		2	μs
		Multicolor (Active area)	2		3.1	μs
		Graphics I (Active area)	2		3.5	μs
		Graphics II (Active area)	2		8	μs

NOTE: Maximum cycle times must be respected at all times for proper operation.

4.4 TIMING REQUIREMENTS OVER FULL RANGES OF RECOMMENDED OPERATING CONDITIONS FOR TMS9118/9128/9129 (Continued)

External Components (Figure 4-5)

	PARAMETER	MIN	TYP	MAX	UNIT
f_{ext}	External source frequency	10.738098	10.738635	10.739172	MHz
t_r	External source rise time		10	15	ns
t_f	External source fall time		10	15	ns
t_{wH}	External source high-level pulse duration	42	47	52	ns
t_{wL}	External source low-level pulse duration	42	47	52	ns
t_d	External source phase delay from XTAL1 falling edge to XTAL2 falling edge	42	47	52	ns
R_L	External load resistor on COMVID, Y, R-Y, B-Y	470			Ω



NOTE: All measurements are made at 10% and 90% points.

FIGURE 4-5 – EXTERNAL CLOCK TIMING WAVEFORM

4.4 TIMING REQUIREMENTS OVER RECOMMENDED SUPPLY VOLTAGE RANGE AND OPERATING FREE-AIR TEMPERATURE RANGE FOR TMS9118/9128/9129 (Concluded)

VRAM Early Write and Read Cycles (Figures 4-6 and 4-7)

PARAMETER		ALT. SYMBOL	MIN	TYP	MAX	UNIT
$t_{c(rd)}$	Read cycle time†	t_{RC}	370	372		ns
$t_{c(W)}$	Write cycle time	t_{WC}	370	372		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharged time)	t_{CP}	85	125		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	195	235	270	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharged time)	t_{RP}	120	135		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low†	t_{RAS}	200	230	270	ns
$t_{w(W)}$	Write pulse duration†	t_{WP}	140	180		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	15	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0	25		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	10	40		ns
$t_{su(D)}$	Data setup time with respect to $\overline{CAS}$ low	t_{DS}	0	25		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0	35		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	240	280		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	145	185		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	190	230		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	25	45		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	275	315		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	100	140		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	185	230		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	145	185		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	135	175		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	40	80		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	95	140		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	195	240		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	280	320		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0	40		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	120	140		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	t_{RCD}	40	80	120	ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	10	40		ns
t_{rf}	Refresh time interval	t_{REF}	4	4		ns
$t_{a(C)}$	Access time after $\overline{CAS}$ low	t_{CAC}			140	ns
$t_{a(R)}$	Access time after $\overline{RAS}$ low	t_{RAC}			230	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	t_{OFF}	0			ns

† All cycle times assume t_t = 5 ns.

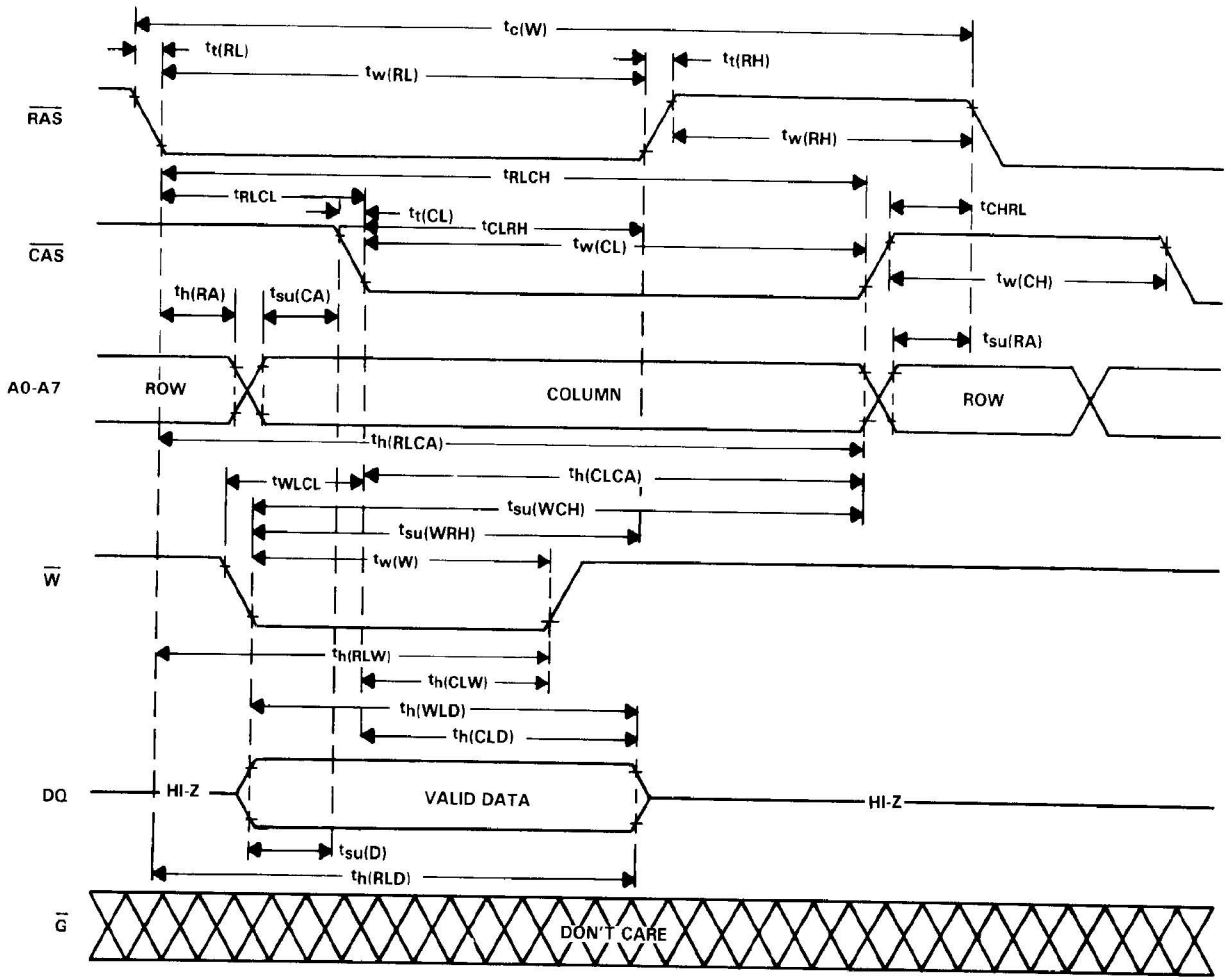
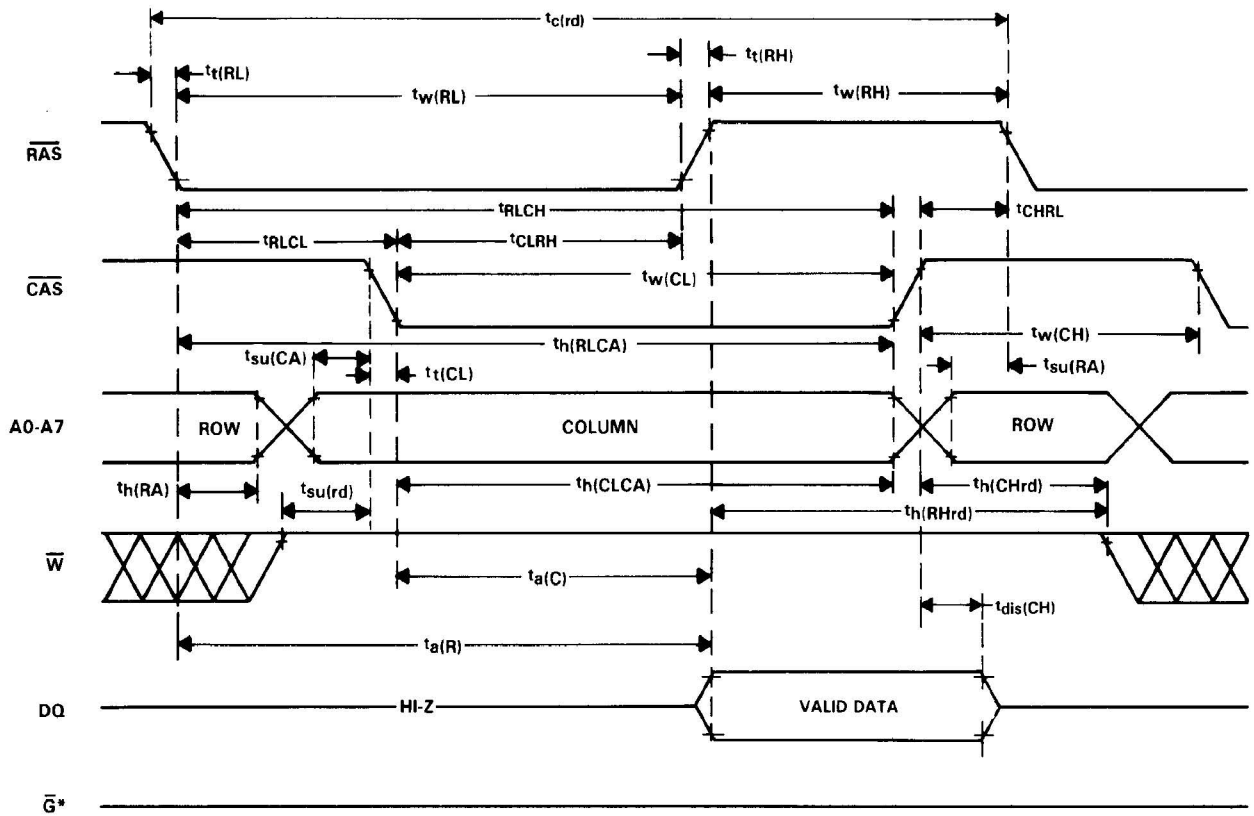


FIGURE 4-6 – VRAM EARLY WRITE CYCLE



* $\overline{G}$ Will be held at V_{SS} (GND) for all operations.

FIGURE 4-7 – VRAM READ CYCLE

4.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (TMS9118/9128/9129)

CPU-VDP Interface (Figure 4-4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{a(CSR)}$	Data access time from $\overline{CSR}$ low	C_L = 100 pF		100	150	ns
$t_{dis(CSR)}$	Data disable time after $\overline{CSR}$ high			65	100	ns
$t_{dis(A)}$	Data disable time from address changes			0		ns
f_{CPUCLK}	CPUCLK output frequency		0.33 f_{ext} − 100Hz	0.33 f_{ext}	0.33 f_{ext} + 100Hz	MHz
d_{CPU}	CPU duty cycle		40	45	50	%

TMS9118 Composite Video Output (Figures 4-8 and 4-9)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{f1}	Fall time, V_{BLACK} to V_{SYNC}	R_L = 470 Ω, C_L = 75 pF		10		ns
$t_{w(HS)}$	Pulse duration, horizontal sync			4.84		µs
t_{r1}	Rise time, V_{SYNC} to V_{BLACK}			20		ns
t_{HS-CB}	Delay time, horizontal sync to color burst			372		ns
$t_{w(CB)}$	Pulse duration, color burst			2.61		µs
t_{CB-LB}	Delay time, color burst to left border			1.49		µs
t_{r2}	Rise time, V_{BLACK} to V_{WHITE}			60		ns
$t_{w(LB)}$	Pulse duration, left border video			2.42		µs
t_{f2}	Fall time, V_{WHITE} to V_{BLACK}			110		ns
$t_{w(AD)}$	Pulse duration, active display area			47.68		µs
$t_{w(RB)}$	Pulse duration, right border video			2.79		µs
t_{RB-HS}	Delay time, right border to horizontal sync			1.49		µs
t_{VFB}	Vertical front porch blanking time			191.1		µs
t_{VS}	Vertical sync time			191.1		µs
t_{VBB}	Vertical back porch blanking time			828		µs
t_{ABA}	Active plus border area time			15.48		µs

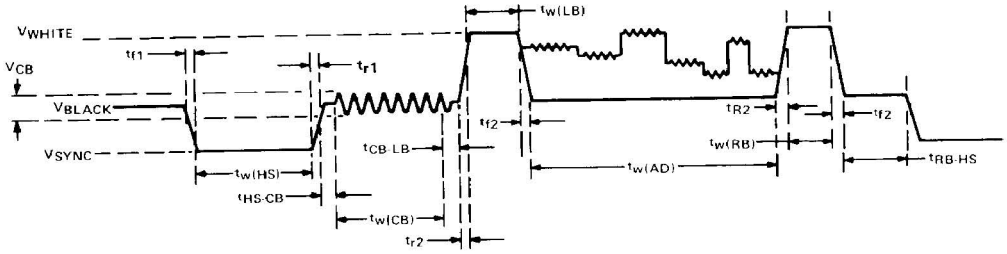
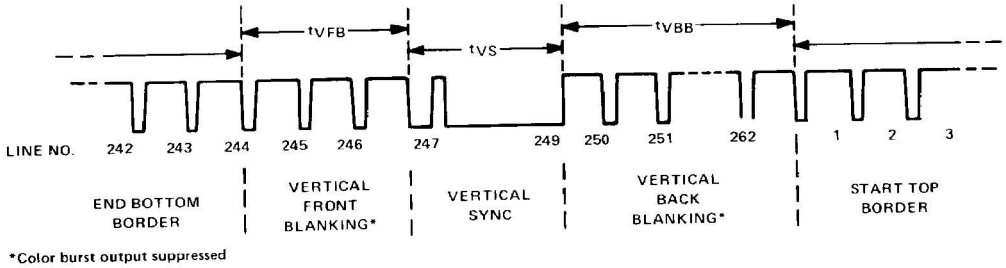


FIGURE 4-8 – TMS9118 COMVID HORIZONTAL TIMING



*Color burst output suppressed

FIGURE 4-9 – TMS9118/9128 VERTICAL TIMING

4.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (Concluded)

TMS9128/9129 Y, R-Y, B-Y Outputs (Figures 4-10 through 4-13)

PARAMETER		TEST CONDITIONS	TMS9128	TMS9129	UNIT
			TYP	TYP	
t_{f3}	Fall time, V_{BLACK} to V_{SYNC}	R_L = 470 Ω, C_L = 75 pF	100	100	ns
$t_{w(HS)}$	Pulse duration, horizontal sync		4.84	4.66	μs
t_{r3}	Rise time, V_{SYNC} to V_{BLACK}		150	150	ns
$t_{w(BP)}$	Pulse duration, back porch		4.47	5.77	μs
$t_{w(LB)}$	Pulse duration, left border		2.42	2.42	μs
$t_{w(PI)}$	Pulse duration, pixel		186.24	186.24	ns
$t_{w(H)}$	Pulse duration, horizontal line		63.695	63.695	μs
$t_{w(AD)}$	Pulse duration, active display area		47.68	47.68	μs
t_{r4}	Rise time, V_{BLACK} to V_{WHITE}		75	75	ns
t_{f4}	Fall time, V_{WHITE} to V_{BLACK}		50	50	ns
$t_{w(RB)}$	Pulse duration, right border		2.79	1.68	μs
$t_{w(FP)}$	Pulse duration, front porch		1.49	1.49	μs
t_{r5}	Rise time, $V_{NO\ COLOR}$ to $V_{POS\ COLOR\ BURST}$		150	150	ns
$t_{w(CB)}$	Pulse duration, pos color burst		2.61	2.42	μs
t_{f5}	Fall time, $V_{POS\ COLOR\ BURST}$ to $V_{NO\ COLOR}$		100	100	ns
$t_{w(CB-LB)}$	Blank time, color burst to left border		1.49	2.42	μs
t_{f6}	Fall time, $V_{NO\ COLOR}$ to $V_{NEG\ COLOR\ BURST}$		100	100	ns
t_{r6}	Rise time, $V_{NEG\ COLOR\ BURST}$ to $V_{NO\ COLOR}$		150	150	ns
$t_{w(VS)}$	Pulse duration, vertical sync		559	4660	ns
t_{VFB}	Vertical front blanking		191.09	191.09	μs
t_{VS}	Vertical sync		195.93	195.74	μs
t_{VBB}	Vertical back blanking		823.20	1210	μs
t_{ABA}	Active area plus border area total		15.48	18.34	ms
t_V	Vertical time		16.69	19.94	ms

NOTE: Fall times depend on external pull-down resistor.

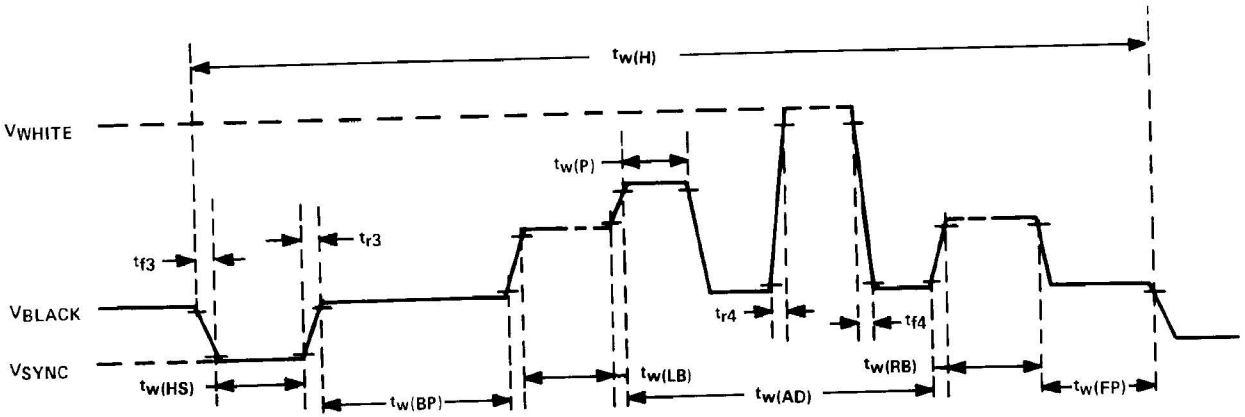
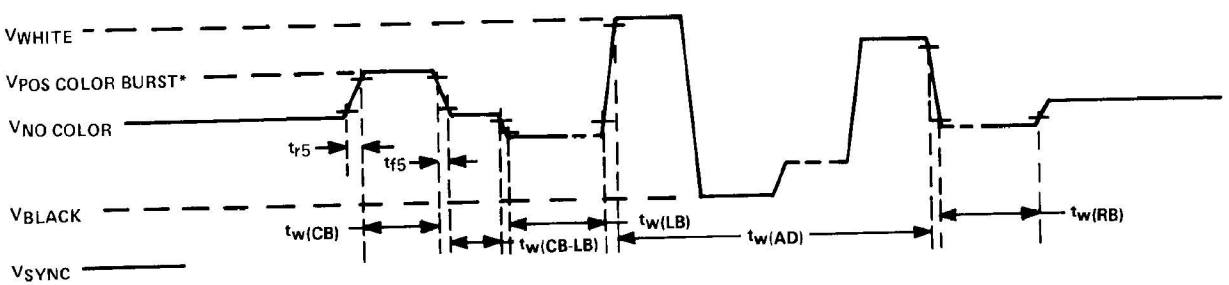


FIGURE 4-10 – TMS9128/9129 Y HORIZONTAL TIMING



* Absent for the TMS9128

FIGURE 4-11 – TMS9128/9129 R-Y HORIZONTAL TIMING

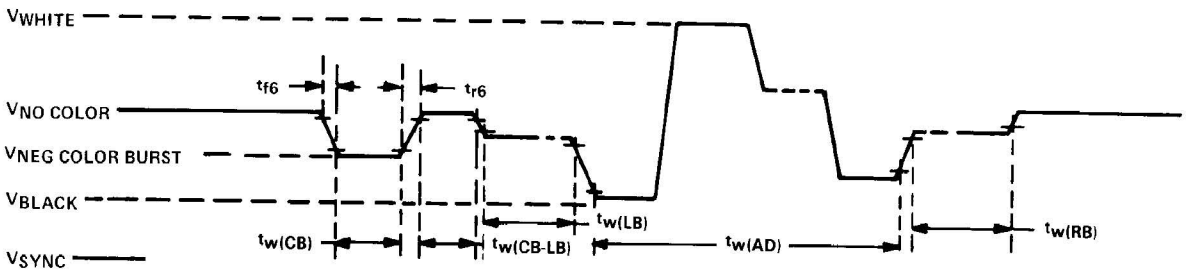


FIGURE 4-12 – TMS9128/9129 B-Y HORIZONTAL TIMING

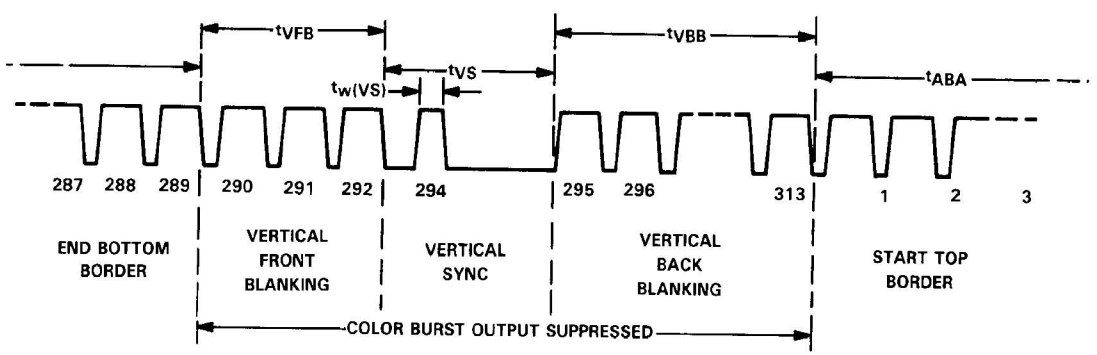


FIGURE 4-13 – TMS9129 VERTICAL TIMING

4.6 MECHANICAL DATA

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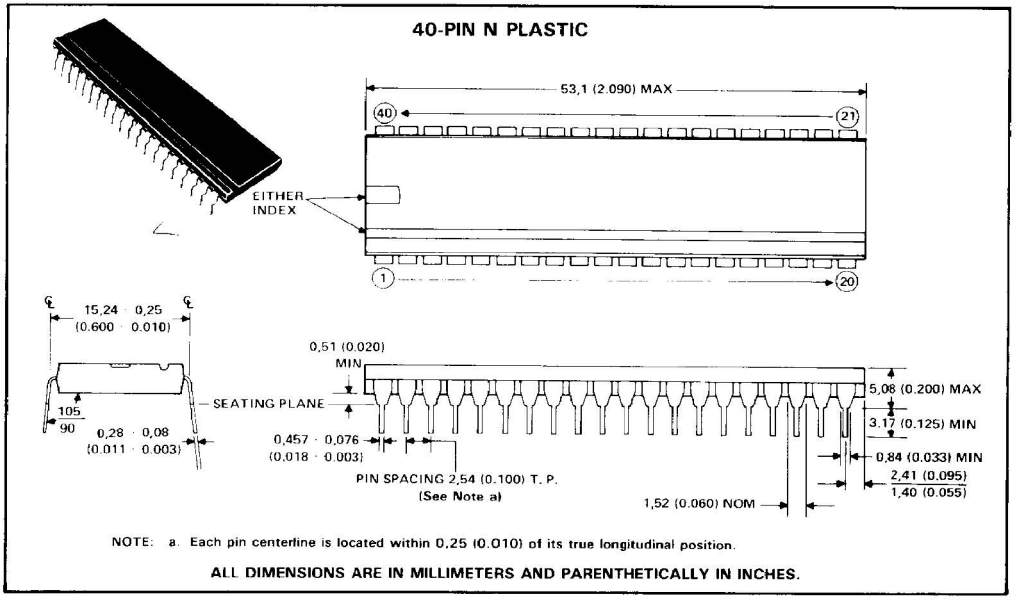

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.